REMARKS

Applicant has the following response to the Office Action of July 20, 2006. Except as discussed in detail below, Applicant is merely amending the claims to correct minor matters in form.

Applicant will address each of the Examiner's objections and rejections in the order in which they appear in the Office Action.

Drawings

In the Office Action, the Examiner objects to the drawings and requests that Figure 2 be labeled "Prior Art." Applicant has now done so and respectfully requests that this objection be withdrawn.

Specification

The Examiner also objects to the specification at page 7, line 25 to page 8, line 11 for informalities therein. In particular, the Examiner states that this section refers to Figures 5A-5E but should reference Figures 6A-6E.

Applicant is making the Examiner's suggested correction herein. Therefore, it is respectfully requested that this objection be withdrawn.

Claim Rejections - 35 USC §112

The Examiner also rejects Claims 7 and 9 as lacking an antecedent basis for "said plurality of gate lines" and "said plurality of source lines."

Applicant has amended these claims to correct this informality. Accordingly, it is respectfully requested that this rejection be withdrawn.

Claim Rejections - 35 USC §103

The Examiner also rejects Claims 1-12 under 35 USC §103(a) as being unpatentable over Kaneko et al. (JP 2000-047255) in view of Koyama (US 2001/0040565). This rejection is respectfully traversed.

While Applicant traverses this rejection, in order to advance the prosecution of this application, Applicant is amending independent Claims 1, 3, 7 and 9 to recite the features of "a testing circuit comprising an input portion, an output portion, and a portion wherein a plurality of NAND circuits is connected in series so that an output of one of the plurality of NAND circuits is directly connected to one of input of the another one of the plurality of NAND circuits" and "a number of the plurality of data signal lines is equal to a number of the plurality of NAND circuits." These features are supported by, for example, Fig. 1A, Fig. 3A and page 4, lines 20-21 of the specification of the present application.

In the Office Action, the Examiner alleges that "it would have been obvious to 'one of ordinary skill' in the art at the time the invention was made to replace the AND circuits taught by Kaneko et al. with the NAND circuits with the buffers comprising 3 inverters taught by Koyama such that the logical equivalent of the AND circuit would be kept while using NAND circuits in order to provide a buffer before the result from the NAND circuit is output to the next NAND circuit." Applicant respectfully disagrees and submits that even if one combined the references as proposed by the Examiner, one still would not arrive at the claimed invention.

More specifically, when Applicant tried to replace the AND circuit taught by Kaneko with the NAND circuits with the buffers comprising 3 inverters taught by

Koyama (in accordance with the Examiner's proposal), Fig. A shown below is believed to be the result.[1]

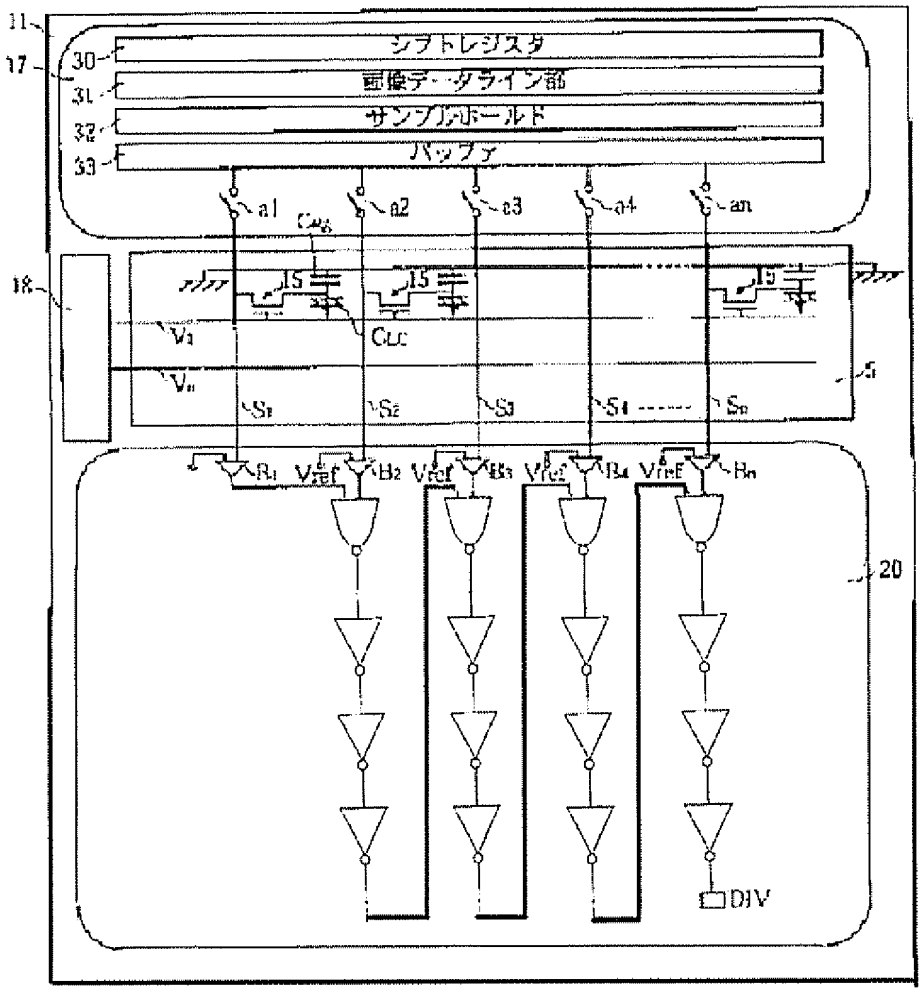
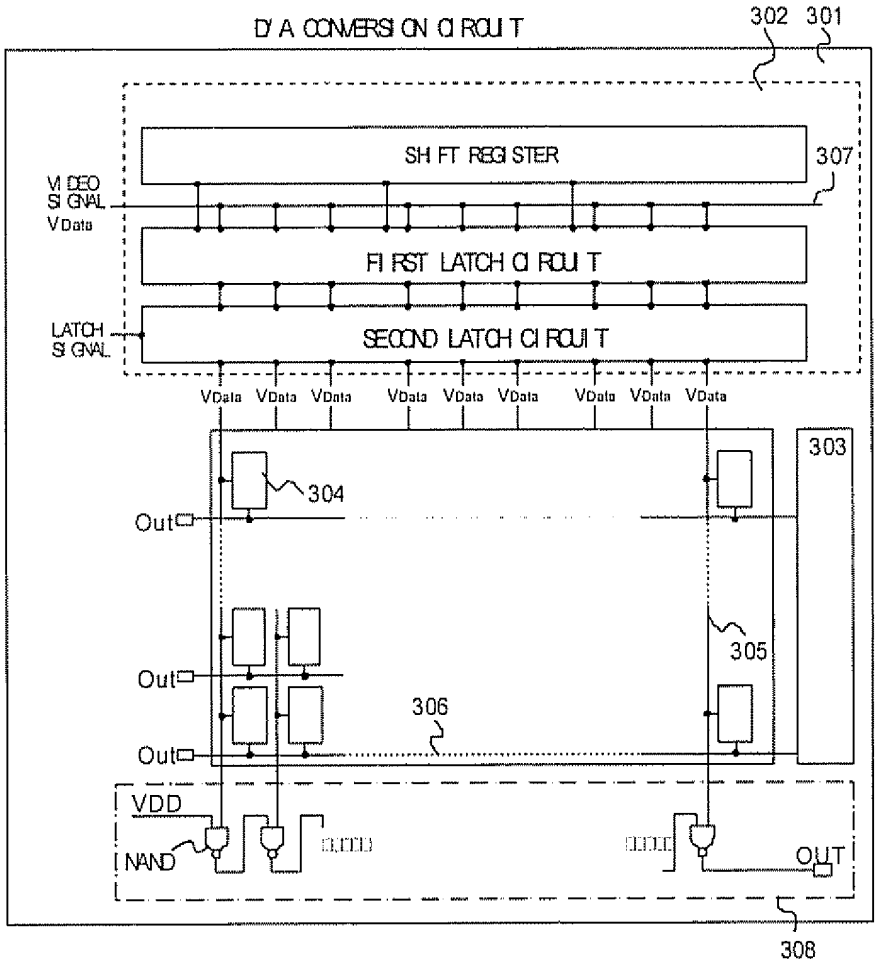


Fig. A

For comparison, Applicant is including below a copy of Fig. 3A of the present application:

[1] Applicant does not admit that this combination is proper. Applicant is presenting Fig. A for illustration purposes only, to show that even if these references were combined, the combination would still be insufficient.

FIG. 3A



Comparing Fig. 3A of the present application and Fig. A (Examiner's alleged combination of Kaneko with Koyama), two differences are readily apparent.

First, in Fig. 3A, the NAND circuits are connected in series so that an output of one of the plurality of NAND circuits is directly connected to one of input of the another one of the plurality of NAND circuits, as recited in the amended claims, and no buffer is provided before the result from the NAND circuit is output to the next NAND circuit. In contrast, in Fig. A, buffers comprising 3 inverters are provided, and therefore an output of one of the plurality of NAND circuits is not directly connected to one of input of the another one of the plurality of NAND circuits.

Second, in Fig. 3A, the number of the plurality of data signal lines is equal to the number of the plurality of NAND circuits, as recited in the amended claims. In contrast, in Fig. A, the number of the plurality of data signal lines is larger than that of the plurality of NAND circuits.

Thus, even if these references are combined and AND is replaced with NAND, the combination still fails to disclose or suggest the device or method of independent Claims 1, 3, 7, and 9 and these independent claims and the claims dependent thereon are patentably distinguishable over the cited references. Accordingly, it is respectfully requested that this rejection be withdrawn.

Information Disclosure Statement

Applicant is submitting an information disclosure statement (IDS) herewith. It is respectfully requested that this IDS be entered and considered prior to the issuance of any further action on this application.

Conclusion

It is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any fee should be due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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